REMARKS

Claims 1-20 are all the claims presently pending in the application. Claim 1 is amended to more clearly define the invention. Claims 1 and 10 are independent.

These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicants also note that, notwithstanding any claim amendments herein or later during prosecution, Applicants' intent is to encompass equivalents of all claim elements.

Claims 1-20 stand rejected under 35 U.S.C. 112, second paragraph. Claims 1-2 stand rejected under 35 U.S.C. 102(b) as being anticipated by the Yamashita, et al. reference (USPN 5,506,516). Claims 1-20 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 7-9, 11, 13 and 15 of USPN 6,437,596

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

A first exemplary embodiment of the claimed invention, as defined by independent claim 1, is directed to a display system that includes an array of pixel cells formed on a substrate. Each pixel cell being coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The device includes a first and second transistor formed on the substrate each having a gate electrode and first and second electrodes defining a serpentine channel region there between.

A second exemplary embodiment of the claimed invention, as defined by independent claim 10, is directed to a display system that includes an array of pixel cells formed on a substrate. Each pixel cell being coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. The system further includes a gate line select/hold circuit formed on the substrate and connected to at least one of the plurality of gate lines, a first control pad and a first probe pad, and a data line select/hold circuit formed on the substrate and connected to at least one of said plurality of data lines, a second control pad and a second probe pad. At least one of the gate line select/hold circuit and the data line select/hold circuit includes first and second transistors each having first and second electrodes defining a serpentine channel region.

Conventional display systems include pixel cells formed on a substrate which are each coupled to at least one gate line of a plurality of gate lines formed on the substrate and at least one data line of a plurality of data lines formed on the substrate. An array tester provides a means for testing the cells of such a display system by coupling probes to gate line pads and data line pads that terminate the gate lines and data lines, respectively. In other words, the array tester is coupled directly to each gate line and each data line. However, when the size of such a conventional display system is changed the spacing of the gate lines and/or data lines also changes which requires that the probe fixture of the array tester be modified to accommodate these changes.

By contrast, the present invention includes first and second electrodes in addition to the pixel array which accommodate variations in size and/or resolution without requiring

modification of the probe fixture of the array tester. In other words, the present invention provides a flexible interface between the array under test and the test system. More specifically, in the event that the size of the array under test is changed, the gate line select/hold circuit 17 and/or the data line select/hold circuit 19 and the probe pads associated therewith may be designed such that they align with the spacing of an existing probe fixture, thereby eliminating the high costs associated with redesigning the probe fixture of the array.

Further, each of the first and second transistors have a gate electrode and first and second electrodes defining a serpentine channel region there between. This feature minimizes the time constant required to transfer a charge to/from a capacitive load using the select and hold transistors of the gate line select/hold circuit 17 and the data line select/hold circuit 19 and also reduces the ON resistance of these transistors. The ON resistance of the transistor is proportional to the channel length/width ratio of the transistor. The serpentine channel region minimizes this length/width ratio and, therefore, reduces the ON resistance and the time constant.

II. THE 35 U.S.C. § 112, SECOND PARAGRAPH REJECTION

Before Applicants address the Examiner's rejections under 35 U.S.C. § 112, second paragraph, Applicants respectfully submit that many of the issues raised by the Examiner appear to be the result of confusion on the part of the Examiner which the Applicants respectfully submit could be alleviated and/or avoided had the Examiner read the Applicants' specification.

Should the Examiner continue to experience confusion, Applicants respectfully request that the Examiner contact the undersigned representative to alleviate any further questions or

concerns that the Examiner may have.

The Examiner alleges that claims 1-20 are indefinite. In particular, Examiner Nguyen alleges that it is unclear how the first transistors are interconnected and associated with the gate lines and data lines and that it is unclear how the first transistor and second transistor are interconnected with each other.

Regarding claim 1, Applicants respectfully direct the Examiner's attention to the clear language of claim 1 which clearly states that the first and second transistors are formed on the same substrate as are the gate lines and data lines. Therefore, since claim 1 does not recite nor require interconnection of these transistors it is irrelevant whether or not these transistors are connected.

Regarding claim 4, the Examiner alleges that it is unclear whether the first transistor is the same as the one in claim 3. Applicants respectfully directs that Examiner's attention to the clear language of claim 4 which clearly state "The device of claim 1." Therefore, claim 4 is not relevant to claim 3, and vice-versa. The Examiner's rejection is baseless, illogical, and improper.

Similarly, regarding claim 6, the Examiner alleges that it is unclear whether the first transistor is the same as the one in claim 5. Applicants respectfully directs that Examiner's attention to the clear language of claim 6 which clearly state "The device of claim 1." Therefore, claim 6 is not relevant to claim 5, and vice-versa. The Examiner's rejection is baseless, illogical, and improper.

Regarding claims 8 and 9, the Examiner alleges that it is unclear what a "common electrode" represents. As explained in the specification at, for example, page 22 lines 3-7 and

shown in the drawings at, for example, in Fig. 10(A) in an exemplary embodiment of the present invention the select and hold transistors share a common electrode C. This common electrode C minimizes the space and cost of integrating the select/hold transistor pair with the pixel array.

Regarding claim 10, the Examiner alleges that it is unclear what "a first control pad," "first probe pad," "second control pad" and "second probe pad" represent. Applicants respectfully direct the Examiner's attention to Figs. 8 and 9, and the specification at, for example, page 19, line 10 - page 20, line 19 where exemplary embodiments are clearly described and illustrated. For example, an exemplary embodiment of a select transistor 801 is shown connected to a hold transistor 803 and a gate line GL. This select/hold transistor pair includes two probe pads 21 and 27, one of which corresponds to a first probe pad and the other one of which corresponds to a second probe pad without further limitation. Similarly, the select/hold transistor pair includes a gate select control pad 25 and a gate hold control pad 28, one of which corresponds to a first control pad and the other one of which corresponds to a second control pad without limitation.

Further regarding claim 10, the Examiner again alleges that it is unclear how the first and second transistors are interconnected and associate with each other. Again, similar to the explanation given above with respect to claim 1, claim 10 does not require interconnection between the first and second transistors. Therefore, since claim 10 does not recite nor require interconnection of these transistors it is irrelevant whether or not these transistors are connected.

Further regarding claim 10 and how the first and second transistors are "associated with each other," claim 10 clearly recites that at least one of the gate line select/hold circuit and the

data line select/hold circuit comprises first and second transistors. Therefore, the association is that at least one of the gate line select/hold circuit and the data line select/hold circuit comprises first and second transistors.

Regarding claim 19, the Examiner alleges that it is unclear whether the data line select hold circuit is connected to the same third control pad as the one in claim 18. Applicants respectfully direct the Examiner's attention to the language of claim 19, which clearly recites "The system of claim 10." Therefore, claim 19 is not dependent from claim 18 and it is irrelevant whether the data line select hold circuit that is recited by claim 19 is connected to the same third control pad as the one in claim 18.

Similarly regarding claim 20, since claim 20 clearly recites "The system of claim 19," claim 20 is not dependent from claim 18 and it is irrelevant whether the data line select hold circuit that is recited by claim 20 is connected to the same third control pad as the one in claim 18.

In view of the foregoing, the Examiner is respectfully requested to withdraw these rejections.

II. THE PRIOR ART REJECTION

Regarding the rejection of claims 1-2, the Examiner alleges that the Yamashita et al. reference teaches the claimed invention. Applicants submit, however, that there are elements of the claimed invention which are neither taught nor suggested by the Yamashita et al. reference.

The Examiner's alleged significance of the Yamashita et al. reference is murky, at best, as

the Office Action did not explain the pertinence of these references to the specific elements which are recited by the claims being rejected, as required by M.P.E.P. § 707.5. Rather, the Examiner merely states that "Yamashita et al (sic) disclose an apparatus for inspecting an array of pixel cells (s) having a plurality of pixel cell (1a) coupled to gate lines (g1,g2,.) and data lines (x1,x2,...xj) and first and second transistors (2b) formed on the substrate." The Examiner's statement completely fails to address the features of the invention which are recited by the claims.

Indeed, even if the Examiner's statement is assumed to be true for the sake of argument, the Examiner has completely failed to allege that the Yamashita et al. reference teaches the features of the present invention as recited by the claims.

The Examiner's allegation ignores the clear language of the claims regarding the first and second transistors "each having a gate electrode and first and second electrodes defining a serpentine channel region there between." Therefore, the Examiner's is clearly deficient on its face.

To further the prosecution of this application, however, Applicants have closely reviewed the Yamashita et al. reference to address the clear differences between the Yamashita et al. reference and the claims.

The Yamashita et al. reference does not teach or suggest the features of the present invention including: a second transistor and first and second electrodes defining a serpentine channel region as recited in independent claim 1.

As explained above, the second transistor is important for providing a flexible interface

between the array under test and the test system. More specifically, in the event that the size of the array under test is changed, the gate line select/hold circuit 17 and/or the data line select/hold circuit 19 and the probe pads associated therewith may be designed such that they align with the spacing of an existing probe fixture, thereby eliminating the high costs associated with redesigning the probe fixture of the array.

Contrary to the Examiner's allegation, the Yamashita et al. reference does not teach or suggest first and second transistors formed on the substrate. In fact, in all five of the embodiments that are disclosed by the Yamashita et al. reference teach in all of their five embodiments (as summarized in table 1 below) that there is only one "analog switch" (2b).

Fig	Embod-iment	Gate Scan Pattern	Gate line control transistors	Control gates on transistors	Data scan pattern	Data line control transistors	Control gates on transistors
1	#1	Sequential	none	none	Sequential	one	one
7	#2	Sequential	none	none	Sequential	one	one
10	#3	Sequential	none	none	Sequential	one	one
13	#4	Sequential	none	none	Sequential	one	one
17	#5	Sequential	none	none	Sequential	one	one

In embodiment 1, the Yamashita et al. reference explains "Specifically, each of the data lines Xj is connected to the video line 2a via a corresponding analog switch 2b," (col. 4, lines 52-54). The Yamashita et al. reference further illustrates in Fig. 1 that there is only one transistor connected to the data line.

In embodiment 2, the Yamashita et al. reference explains "on the other hand, in a case, for example, where a signal is not properly output from the third terminal XX3 of the shift

register 2c, where the corresponding analog switch 2b is not turned on..." (col. 6, lines 46-49). The Yamashita et al. reference further illustrates in Fig. 7 that there is only one transistor connected to the data line.

In embodiment 3, the Yamashita et al. reference illustrates in Fig. 10 that there is only one transistor connected to the data line.

In embodiment 4, the Yamashita et al. reference states that "in another case, for example, where a signal is not properly output from the forth terminal XX4 of the shift register 2c, where the corresponding analog switch 2b is not turned on..." (col. 7, lines 30-33). The Yamashita et al. reference illustrates in Fig. 13 that there is only one transistor connected to the data line.

In the last embodiment 5, the Yamashita et al. reference states that "in another case, for example, where a signal is not properly output from the forth terminal XX4 of the shift register 2c, where the corresponding analog switch 2b is not turned on..." (col. 6, lines 61-64).The Yamashita et al. reference illustrates in Fig. 17 that there is only one transistor connected to the data line.

This is in stark contrast to the claimed invention which recites "a first and second transistor formed on said substate each having a gate electrode and first and second electrodes...", and "wherein a common electrode comprises one of said first and second electrodes of said first transistor and one of said first and second electrodes of said second transistor", ing claims 1 and 2, respectively, and shown, for example, in Fig. 8 and 9 for claims 1 and 2, respectively.

In summary, Yamashita et al. reference discloses having only one transistor ("analog switch 2b") connecting to each corresponding data line of the array, and zero transistors

connecting to each corresponding gate line of the array. In contrast, the claimed invention recites "a first and second transistor formed on said substrate each having a gate electrode and a first and second electrode defining a serpentine channel region there between..." For example, gate and data circuit, shown in Fig. 8 and 9, respectively, includes either "a first (801) and second (803) transistor" or "a first (901) and second (903) transistor." This is clearly described in the present specification at, for example, page 19, lines through 14: " the gate line select/hold circuitry... includes at least one select transistor... and at least one hold transistor..... corresponding to each gate line in the group.."

Secondly, the Yamashita et al. reference discloses a fundamentally different approach to both their data line drive circuitry and scanning line drive circuitry, where all data and gate inspecting lines must be cut (opened) after inspection and before display array operation. Specifically, the Yamashita et al. reference teaches "cutting the inspecting lines from the data (scanning) lines after inspecting the substrate so that said inspecting lines and said inspecting signal input terminals are removed from the inspected substrate" at, for example, col. 9, lines 29-32 to col. 10, lines 5 to 8.

In contrast, the present invention does not require cutting the inspection circuitry. Furthermore, the approach disclosed by the Yamashita et al. reference would not render a working display without cutting the inspecting lines.

The Yamashita et al. reference also does not teach or suggest a serpentine channel region. As explained above, the serpentine channel region is important for minimizing the time constant required to transfer a charge to/from a capacitive load using the select and hold transistors of the

gate line select/hold circuit 17 and the data line select/hold circuit 19 and also reduces the ON resistance of these transistors. The ON resistance of the transistor is proportional to the channel length/width ratio of the transistor. The serpentine channel region minimizes this length/width ratio and, therefore, reduces the ON resistance and the time constant

Indeed, the Yamashita et al. reference does not teach or suggest anything at all regarding the shape of a channel region, let alone first and second electrodes defining a serpentine channel region there between.

Therefore, the Yamashita et al. reference does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection of claims 1-2.

III. THE DOUBLE PATENTING REJECTION

The Office Action rejects claim 1-20 under the judicially created doctrine of obviousness-type double patenting.

Applicants respectfully traverse this rejection.

Contrary to the Examiner's allegation, claims 1-20 of the present application are non-obvious over the claims of U.S. Patent No. 6,437,596. For example, the claims of U.S. Patent No. 6,437,596 do not recite the feature of a serpentine channel region.

Therefore, Applicants respectfully request withdrawal of this rejection.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicants respectfully submit that claims 1-20, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 12/1/02

James E. Howard
Registration No. 39,715

McGinn & Gibb, PLLC
8321 Old Courthouse Rd., Suite 200
Vienna, Virginia 22182
(703) 761-4100
Customer No. 21254